CDB5343: Evaluation Board for CS5343

Features

- Demonstrates Recommended Layout and Grounding Arrangements
- CS8406 Generates S/PDIF and EIAJ-340-Compatible Digital Audio
- Requires Only an Analog Signal Source and Power Supply for a Complete Analog-to-Digital Converter System

Description

The CDB5343 evaluation board is an excellent means for quickly evaluating the CS5343 24-bit, stereo A/D converter. Evaluation requires a digital signal analyzer, an analog source, and a power supply.

Also included is an CS8406 digital audio interface transmitter that generates S/PDIF and EIAJ-340-compatible audio data. The digital audio data is available via RCA phone and optical connectors.

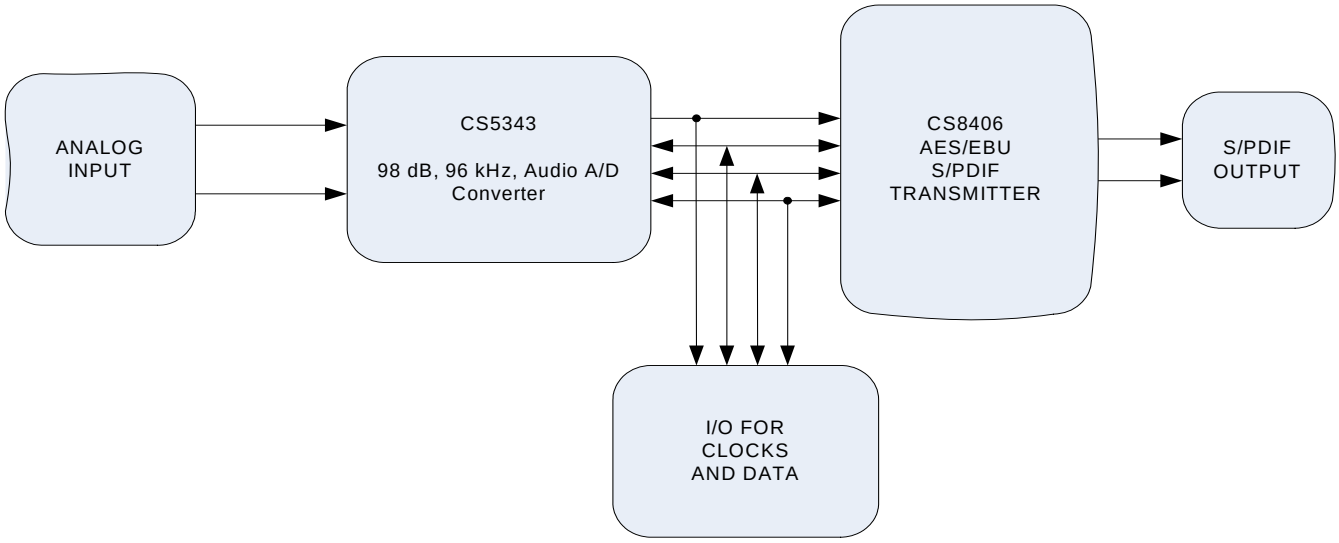

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. SYSTEM OVERVIEW

The CDB5343 evaluation board is an excellent tool for evaluating the CS5343 Analog-to-Digital Converter (ADC). A minimum number of passive components condition the analog input signal prior to the CS5343, and the on-board CS8406 digital audio interface transmitter provides an easy interface to digital audio signal analyzers including the majority of digital audio test equipment. Additionally, the CDB5343 features an interface header (J3) for clock and data I/O.

Figures 19 through Figures 27 show the CDB5343 schematic and layout.

1.1 CS5343

The CS5343 ADC performs stereo 24-bit A/D conversion at sample rates of up to 108 kHz and generates I²S audio format data. Furthermore, in both Master and Slave Modes the CS5343 supports MCLK/LRCK ratios of 256x and 384x. The CS5343 product datasheet contains complete device information.

2. CS8406 DIGITAL AUDIO TRANSMITTER

The CS8406 converts the CS5343 output to a standard S/PDIF data stream. Given an MCLK/LRCK ratio equal to 256x, the CS8406 can operate as clock master or clock slave, but the CS8406 cannot be used with an MCLK/LRCK ratio of 384x on this board. Moreover, by default on this board, the CS8406 accepts only I²S audio format; however, Section 11. on page 8 describes the procedure of configuring the device for Left-Justified audio format. See the CS8406 data sheet for complete device information.

3. CRYSTAL OSCILLATOR

Oscillator Y1 provides an on-board system master clock. The oscillator is mounted in pin sockets, allowing for easy removal or replacement. The board includes a 12.288 MHz crystal oscillator populated at Y1.

4. CLOCK & DATA I/O HEADER

Header J3 makes interfacing to external systems easy. MCLK direction is controlled by switch S1, as is the direction of the sub-clocks, SCLK and LRCK. The header pins associated with MCLK, SCLK, and LRCK can accept 3.3 V or 5 V input signals, but are fixed at 3.3 V when set as outputs. SDOUT is always a 3.3 V output.

4.1 Clock & Data Routing

The user can configure the source and destinations of the clocks required to support the operation of the CS5343. Section 4.1.1 through Section 4.1.3 discuss valid configurations.

4.1.1 MCLK Source

The CS5343 and CS8406 must receive a Master Clock. MCLK can come from either the crystal oscillator installed at Y1 or via header J3. Header J3 can accept a 3.3 V or 5 V logic-level MCLK when configured as an input, but will output MCLK only at 3.3 V when configured as an output.

4.1.2 Sub-Clock Source

SCLK and LRCK comprise the system sub-clocks and must be either provided to, or generated by, the CS5343.

The CS5343 generates sub-clocks when it is set for Master Mode via DIP switch S1. In this scenario, the CS8406 should be set to Slave Mode to receive sub-clocks. Similarly, the “SCLK, LRCK” switch should be closed to direct sub-clocks to the header. The sub-clock output of the J3 header is fixed at 3.3 V.

If the user configures the CS5343 for Slave Mode, the device must receive sub-clocks either from the CS8406 or from an external source via header J3. If the CS8406 is the intended sub-clock source, DIP switch S1 must be set such that the CS8406 is in Master Mode and “SCLK, LRCK” are routed to the header. If both the CS5343 and the CS8406 are set to Slave Mode, DIP switch S1 must indicate that the sub-clocks come “FROM HDR.” Sub-clock input to header J3 may be either 3.3 V or 5 V.

4.1.3 Data Routing

Audio data from the CS5343 SDOUT pin is routed to header J3 and the CS8406. The SDOUT pin of J3 is always a 3.3 V output. The CS5343 produces data in only I²S audio format; therefore the data capture device should be set accordingly.

The CS8406 accepts data in I²S audio format, which it converts to S/PDIF and EIAJ-340-compatible data. This data is available for capture from either the optical connector (J9) or the RCA jack (J6).

5. POWER

Power must be supplied to the evaluation board through the +5 V binding post (J2). The +5 V input must be referenced to the single black binding post ground connector (J1).

WARNING: Please refer to the CS5343 data sheet for allowable voltage levels.

6. GROUNDING AND POWER SUPPLY DECOUPLING

To optimize performance, PCB designs supporting the CS5343 require careful attention to power supply, grounding, and signal routing. Figures 26 and 27 show the basic component/signal interconnect for the CDB5343, and Figure 25 shows the component placement. These figures demonstrate the optimal layout of components used to support the CS5343. For example, these figures show that the decoupling capacitors are located as close to the CS5343 as possible. The layout also shows extensive use of ground plane fill which greatly reduces radiated noise.

7. ANALOG INPUT

The user can input single-ended analog signals via the RCA connectors, J5 and J7. A 2 Vrms single-ended signal into the RCA connectors will drive the CS5343 inputs to full scale (1 Vrms for VA = 5 V). The input network on the CDB5343 was designed to demonstrate that the CS5343 will achieve full performance with a source impedance up to 2.5 kΩ (looking back from the CS5343 inputs) while allowing for 2 Vrms inputs. Another advantage of this circuit is that it provides an input impedance of 10 kΩ, similar to many commercial audio products.

8. CONNECTORS

Table 1 lists the connectors on the CDB5343, the reference designator of each connector, the directionality, and the associated signal.

CONNECTOR	REFERENCE DESIGNATOR	INPUT/OUTPUT	SIGNAL
+5V	J2	INPUT	+5 V power to crystal oscillator and DC voltage regulator
GND	J1	INPUT	Ground connection from the power supply
AINR	J7	INPUT	Analog input right channel
AINL	J5	INPUT	Analog input left channel
Co-axial	J6	OUTPUT	Digital audio (S/PDIF) output
Optical	J9	OUTPUT	Digital audio (S/PDIF) output
I/O HDR	J3	INPUT/OUTPUT	Master Clock, Serial Clock, Left/Right Clock, SDOUT

Table 1. System Connections

9. JUMPER AND SWITCH SETTINGS

The user can fully configure the CDB5343 with a bank of six DIP switches (S1) and a single jumper setting on header J4.

9.1 Jumper J4

This jumper selects the magnitude of VA, either 3.3 V or 5 V. The CS5343 is a single-supply device; therefore the magnitude of VA affects the full-scale analog input voltage as well as the digital I/O voltage. Digital I/O is always fixed at VA, and the full-scale input is nominally 0.56xVA Vpp, as specified in the CS5343 data sheet. If the user selects 5 V, the CS5343 full-scale analog input voltage is 2.82 Vpp (1 Vrms) and the digital I/O is set to 5 V. If 3.3 V is selected, the full-scale analog input voltage is 1.86 Vpp (660 mVrms) and digital I/O is 3.3 V.

9.2 Switch S1

Table 2 shows the available settings for S1 with the default settings.

	OPEN	CLOSED
CS5343	MASTER (default)	SLAVE
CS8406	MASTER	SLAVE (default)
MCLK	FROM HDR	TO HDR (default)
SCLK, LRCK	FROM HDR	TO HDR (default)
SPEED	DSM	SSM (default)
MCLK/LRCK	256x (default)	384x

Table 2. CDB5343 S1 Settings

9.2.1 CS5343

This switch configures the CS5343 for either Master Mode or Slave Mode operation. When set as clock Master, the CS8406 must be set to “Slave” and “SCLK, LRCK” must be set to “TO HDR.” When CS5343 is configured for Slave Mode, the CS8406 must be set for Master Mode, or “SCLK, LRCK” must be set to “FROM HDR.”

Changing the state of this switch while the device is running will have no effect on the CS5343 as it must be reset to detect the change. Reset is accomplished by removing and restoring power to the device. Alternatively, removing and restoring MCLK will initiate a reset of the digital section, which is also sufficient for the CS5343 to detect a change in mode settings.

9.2.2 CS8406

This switch sets the CS8406 for either Master Mode or Slave Mode. In Master Mode, the CS5343 must be configured as a clock slave and “SCLK, LRCK” set to “TO HDR.” In Slave Mode, either the CS5343 can be set to Master Mode or the user can set the “SCLK, LRCK” switch to “FROM HDR.”

9.2.3 MCLK

MCLK can either come from the header, as selected by “FROM HDR,” or from the on-board crystal oscillator (Y1) as selected by “TO HDR.”

9.2.4 SCLK, LRCK

The sub-clocks, SCLK and LRCK, are either produced on board by the CS5343 or the CS8406 or produced externally. If generated by an external device, this switch must be set to “FROM HDR.” If the CS5343 or CS8406 generate the sub-clocks, this switch must be set to “FROM HDR.”

9.2.5 SPEED

The CS5343 can operate in Single-Speed Mode (SSM) or Double-Speed Mode (DSM) as described in the CS5343 product datasheet.

In Master Mode, the CS5343 defaults to SSM based on an internal 100 kΩ pull-up resistor from the LRCK pin to VA. Setting the “SPEED” switch to “DSM” will place a 10 kΩ pull-down resistor between LRCK and GND to select Double-Speed Mode. Because the CS5343 determines its Master Mode speed based on start-up options, the speed mode cannot be toggled during operation. To change the speed in Master Mode, the device must be reset by removing and restoring power or removing and restoring MCLK.

This switch also configures the MCLK/LRCK ratio for the CS8406. Selecting SSM configures the CS8406 for a 512x MCLK/LRCK ratio while DSM sets an MCLK/LRCK ratio of 256x. In this design, the CS8406 cannot support of a 384x MCLK/LRCK ratio.

9.2.6 MCLK/LRCK Ratio

This switch will configure the CS5343 for either a 256x MCLK/LRCK ratio or a 384x MCLK/LRCK ratio in Master Mode. In Slave Mode the CS5343 auto-detects the MCLK/LRCK ratio; therefore this configuration step is unnecessary in Slave Mode. In Master Mode, selection of this parameter is performed via a start-up option. An internal 100 kΩ pull-up resistor from the SCLK pin to VA will select 256x by default. An external 10 kΩ pull-down resistor from the SCLK pin to GND will select an MCLK/LRCK ratio of 384x.

Typical applications that use a 384x MCLK/LRCK ratio derive a 48 kHz LRCK from a 18.384 MHz MCLK. Deriving MCLK from the included 12.288 MHz crystal oscillator will result in a sample rate of 32 kHz.

The CS8406 is not configured to support a 384x MCLK/LRCK ratio in this design; therefore analysis in this mode must be performed by retrieving data through the interface header (J3).

10.RESET

The CS5343 features Power-On Reset which means that performing a full reset of the CS5343 requires a power-cycling the device. On the CDB5343, this can be accomplished with by removing and restoring the power-supply or by removing and restoring the jumper on J3. Alternatively, removing and restoring MCLK to the device will effect a reset of just the digital portion of the device. The device enters Power-Down Mode when MCLK is removed and draws less current.

11.EVALUATING THE CS5344

The CDB5343 comes with only the CS5343 ADC installed, but some users may want to evaluate the pin-compatible CS5344 ADC. The two devices perform equivalently, but the CS5344 produces only Left-Justified audio format data; whereas the CS5343 creates only I²S audio format data. By following the four easy steps listed below, the user can modify the CDB5343 to accommodate the CS5344.

- *Step 1:* Remove CS5343 populated at U6
- *Step 2:* Install CS5344 at U6
- *Step 3:* Remove 0 Ω resistor populated at R36 (this resistor selects I²S Audio Format for the CS8406)
- *Step 4:* Install 0 Ω resistor at R43 (this resistor selects LJ Audio Format for the CS8406)

12.PERFORMANCE PLOTS

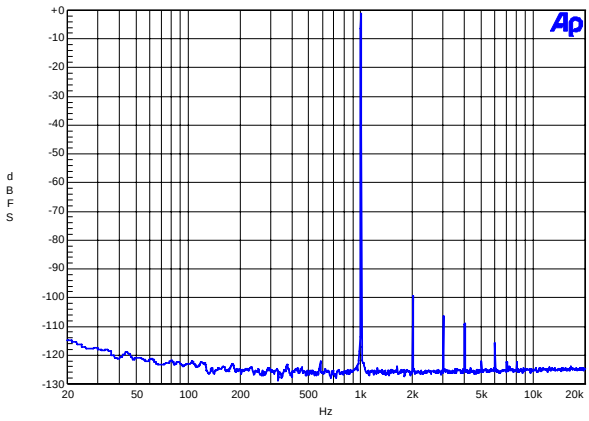


Figure 1. FFT (-1 dB 48 kHz)

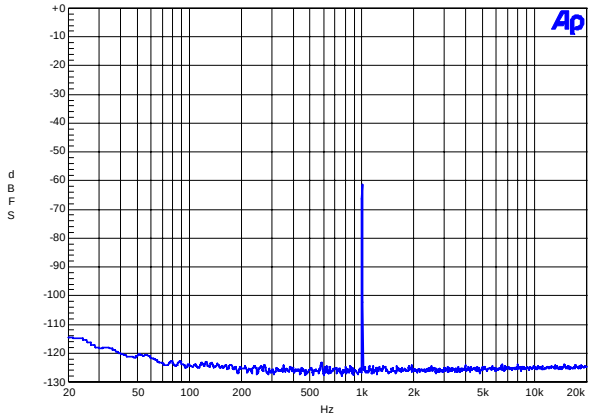


Figure 2. FFT (-60 dB, 48 kHz)

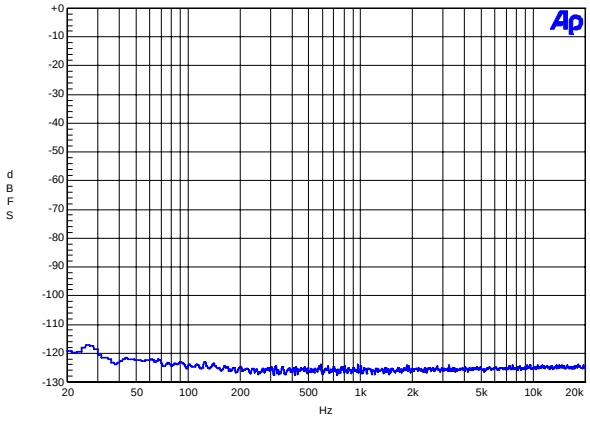


Figure 3. FFT (48 kHz, No Input)

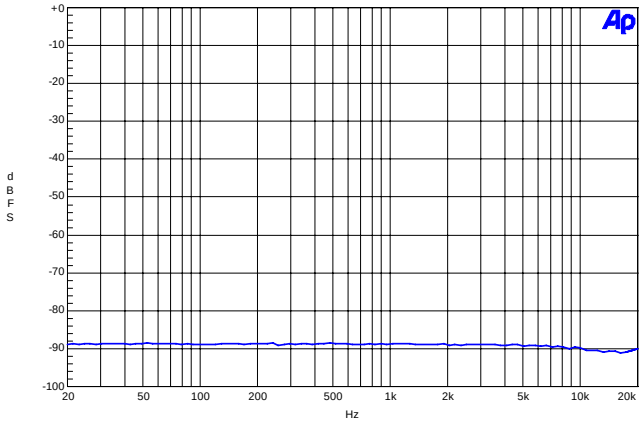


Figure 4. 48 kHz, THD+N vs. Input Freq

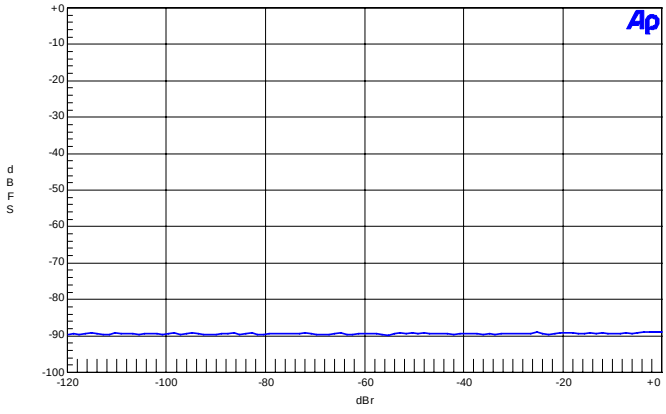


Figure 5. 48 kHz, THD+N vs. Level

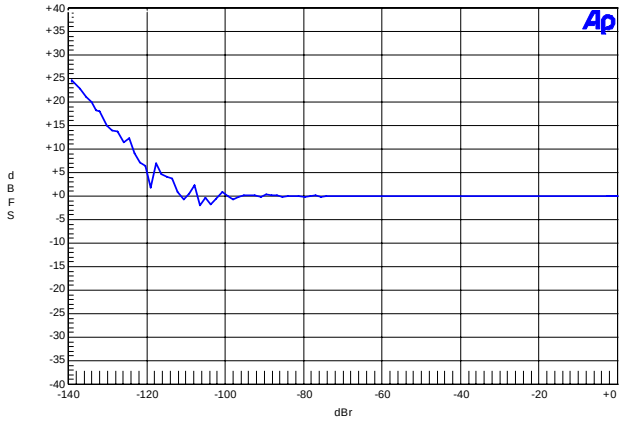


Figure 6. 48 kHz, Fade-to-Noise Linearity

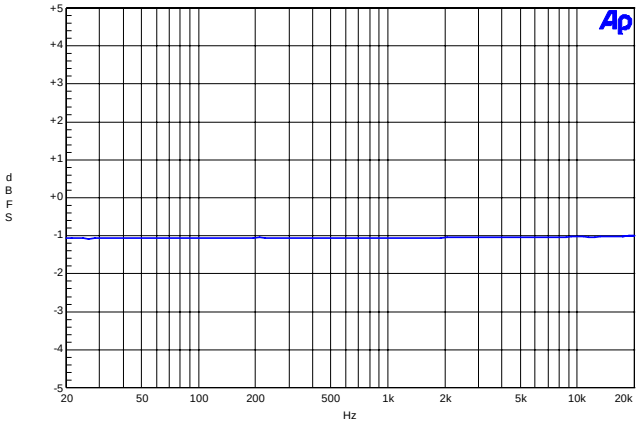


Figure 7. 48 kHz, Frequency Response

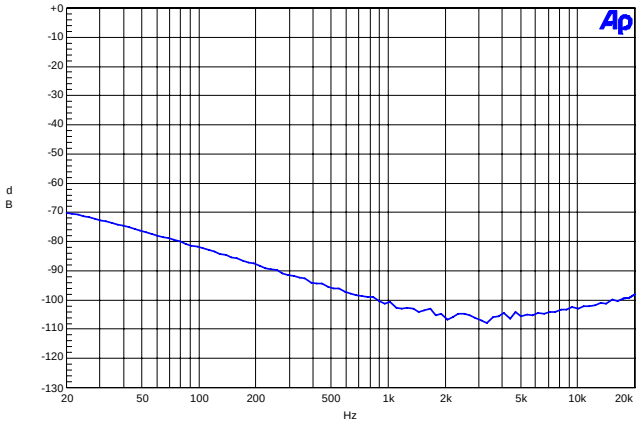


Figure 8. 48 kHz, Crosstalk

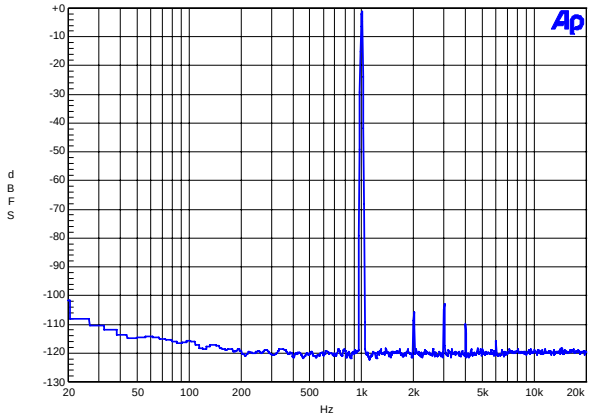


Figure 9. FFT (-1 dB 96 kHz)

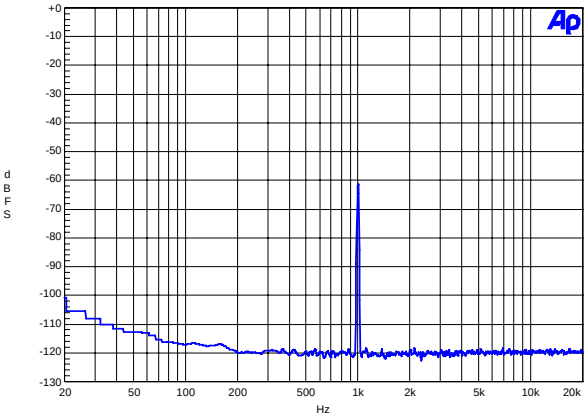


Figure 10. FFT (-60 dB, 96 kHz)

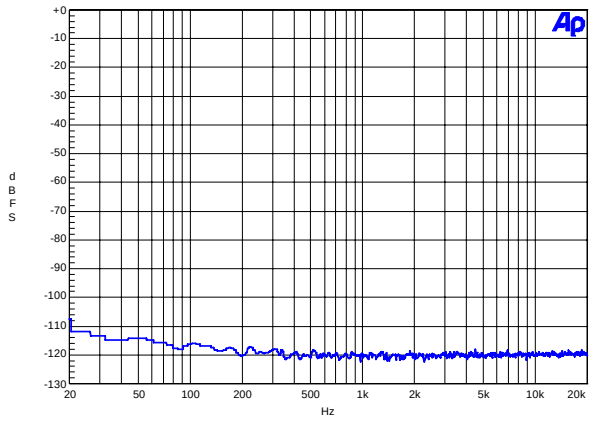


Figure 11. FFT (96 kHz, No Input)

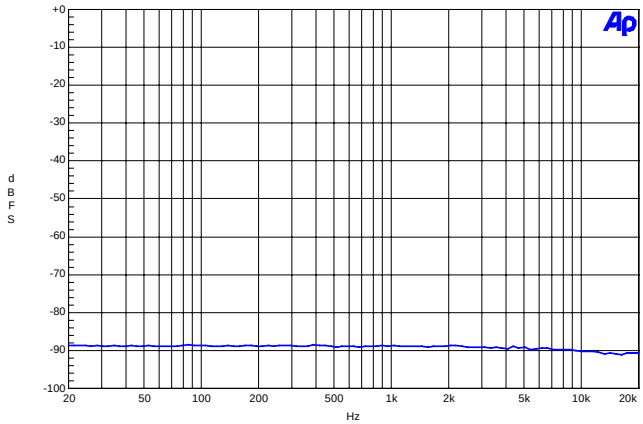


Figure 12. 96 kHz, THD+N vs. Input Freq

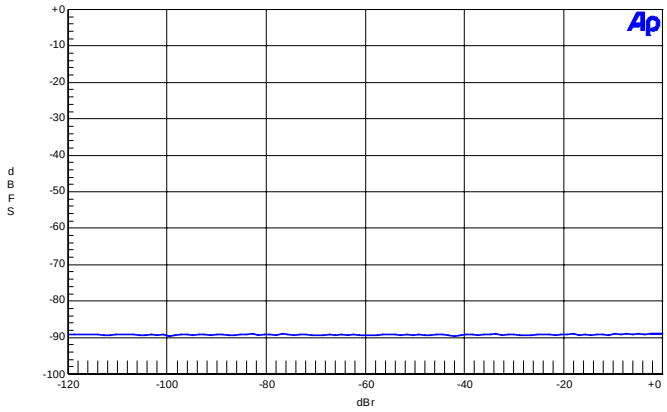


Figure 13. 96 kHz, THD+N vs. Level

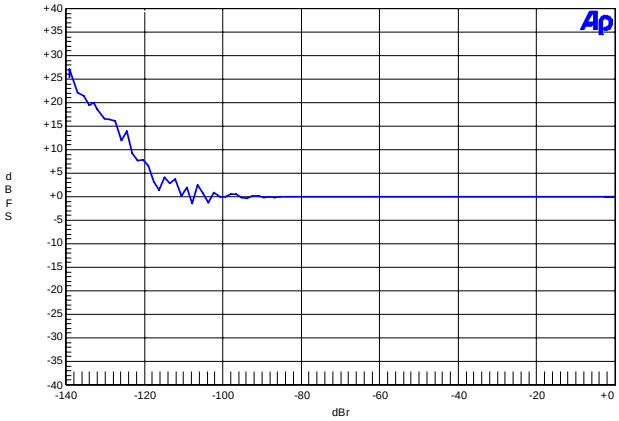


Figure 14. 96 kHz, Fade-to-Noise Linearity

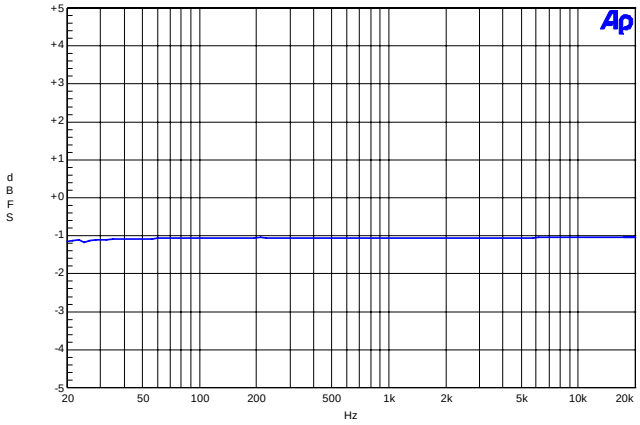


Figure 15. 96 kHz, Frequency Response

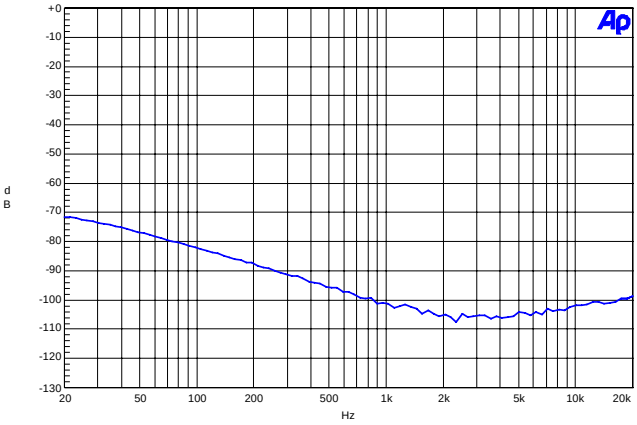
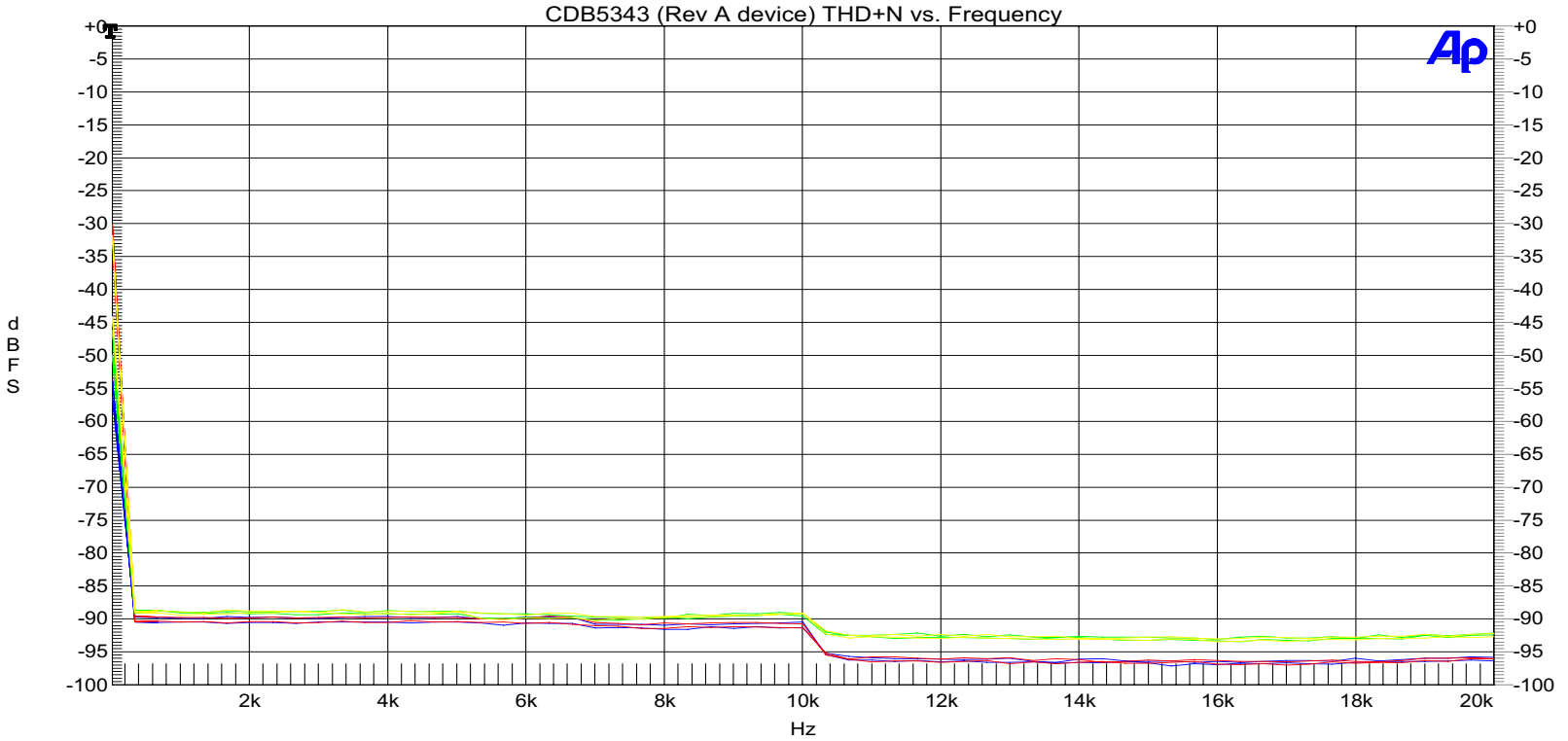


Figure 16. 96 kHz, Crosstalk

13.CDB PERFORMANCE CURVES

13.1 Total Harmonic Distortion + Noise (THD+N)

Figure 17 shows typical THD+N performance of the CS5343 installed on the CDB5343. Performance curves are displayed for each channel with the CS5343 running at Single-Speed in both Master and Slave Modes and for VA voltages of both +3.3 V and 5 V.

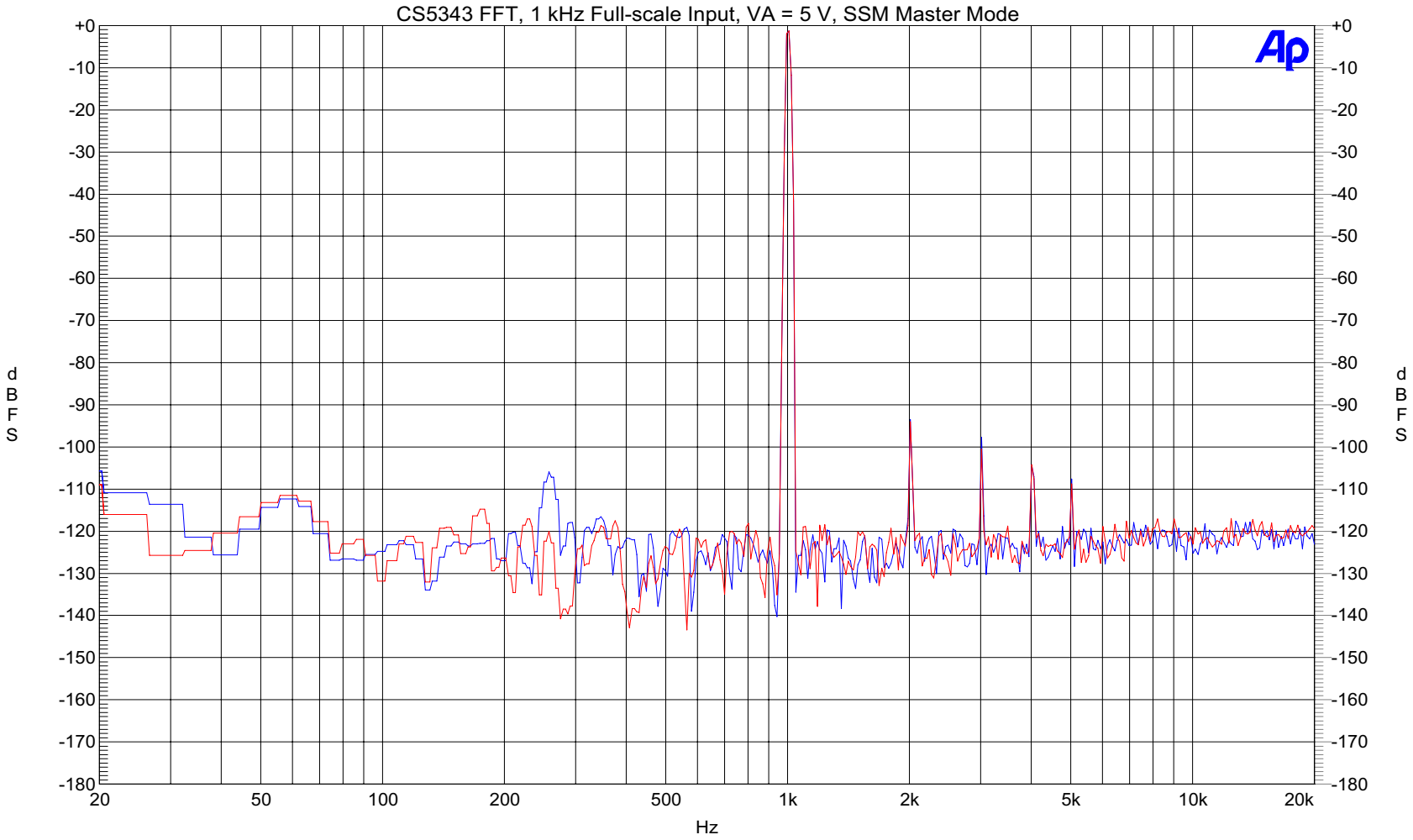


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	1	DSP Anlr.THD+N Ampl A	Left	5V Master SSM 256x
1	2	Blue	Solid	1	DSP Anlr.THD+N Ampl B	Right	5V Master SSM 256x
2	1	Red	Solid	1	DSP Anlr.THD+N Ampl A	Left	5V Slave SSM 256x
2	2	Red	Solid	1	DSP Anlr.THD+N Ampl B	Right	5V Slave SSM 256x
3	1	Green	Solid	1	DSP Anlr.THD+N Ampl A	Left	3.3 V Slave SSM 256x
3	2	Green	Solid	1	DSP Anlr.THD+N Ampl B	Right	3.3 V Slave SSM 256x
4	1	Yellow	Solid	1	DSP Anlr.THD+N Ampl A	Left	3.3 V Slave SSM 256x
4	2	Yellow	Solid	1	DSP Anlr.THD+N Ampl B	Right	3.3 V Slave SSM 256x

Figure 17. CDB5343 THD+N Performance

13.2 FFTIm

Figure 18 shows a typical FFT of the output from the CS5343 on the CDB5343 with a 2 Vrms, 1 kHz sinewave input. For this plot, the device was configured for Single-Speed Mode with VA = 5 V.



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	1	Fft.Ch.1 Ampl	Left	
1	2	Red	Solid	1	Fft.Ch.2 Ampl	Right	

Figure 18. FFT from CDB5343 Output

14.CDB SCHEMATICS

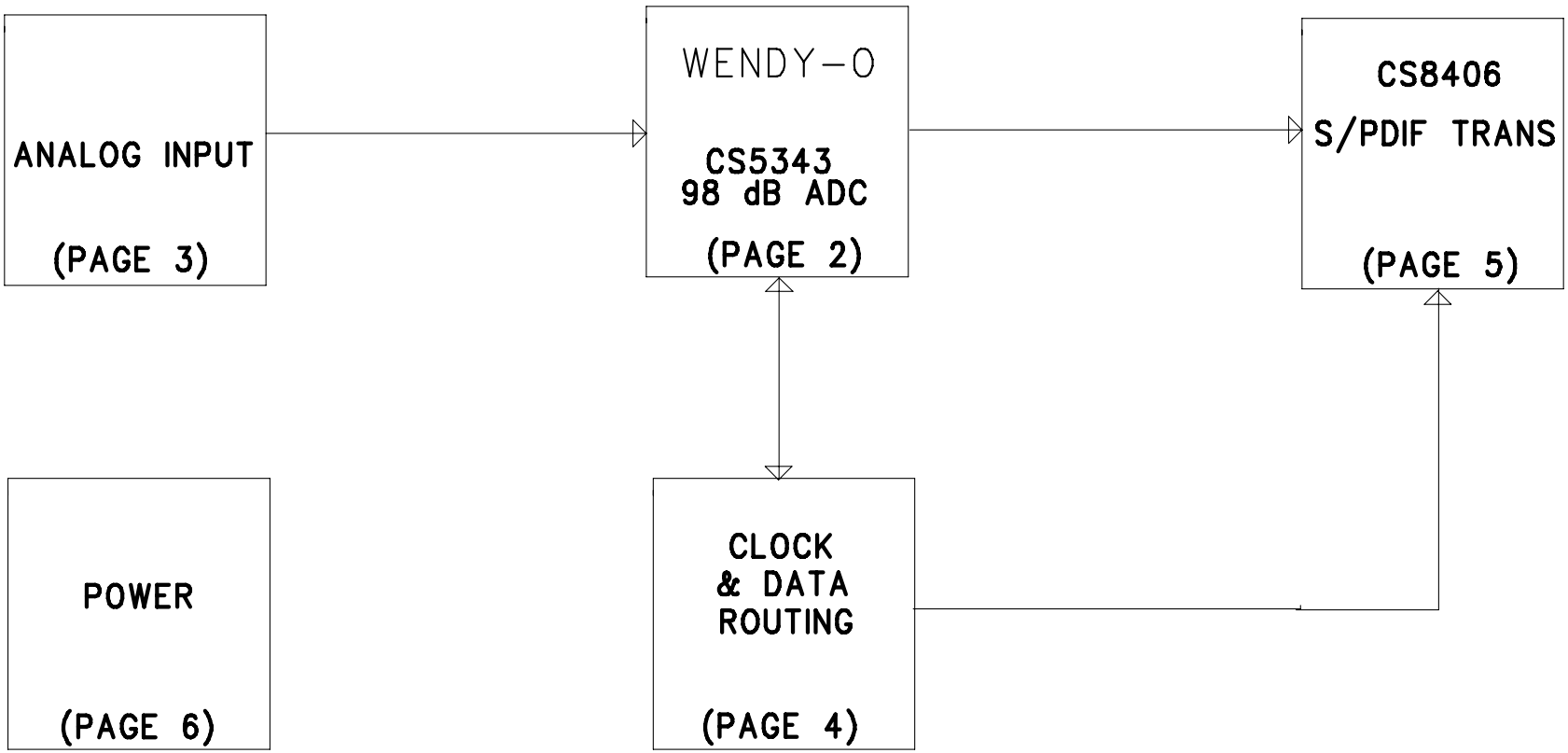
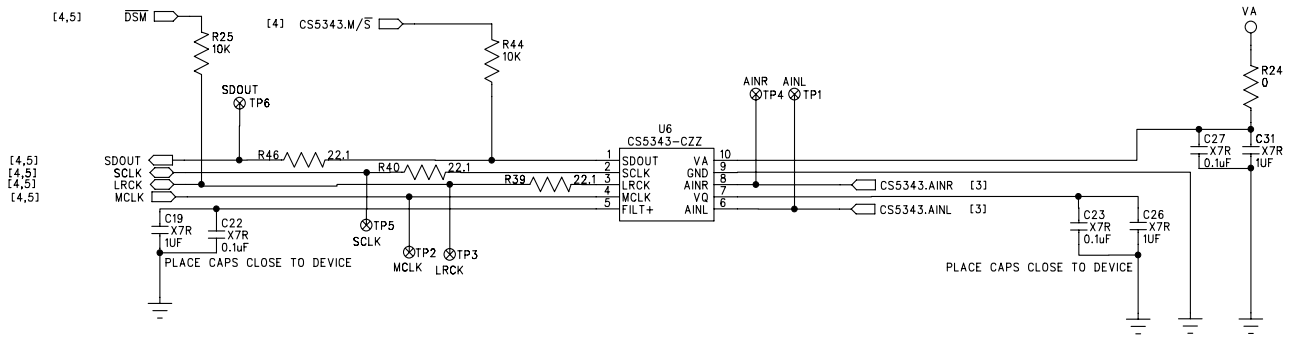


Figure 19. CDB Block Diagram



CS5343 96 kHz STEREO CODEC

Figure 20. CS5343 Analog-to-Digital Converter

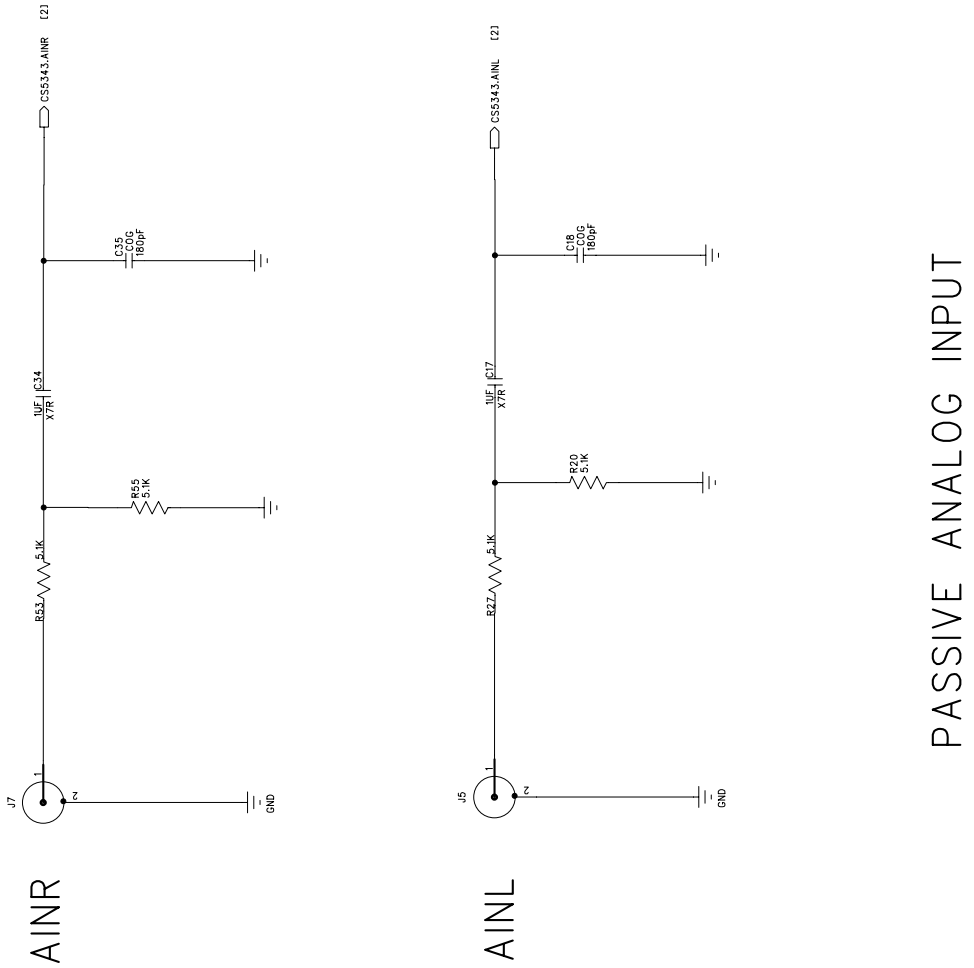


Figure 21. Analog Input

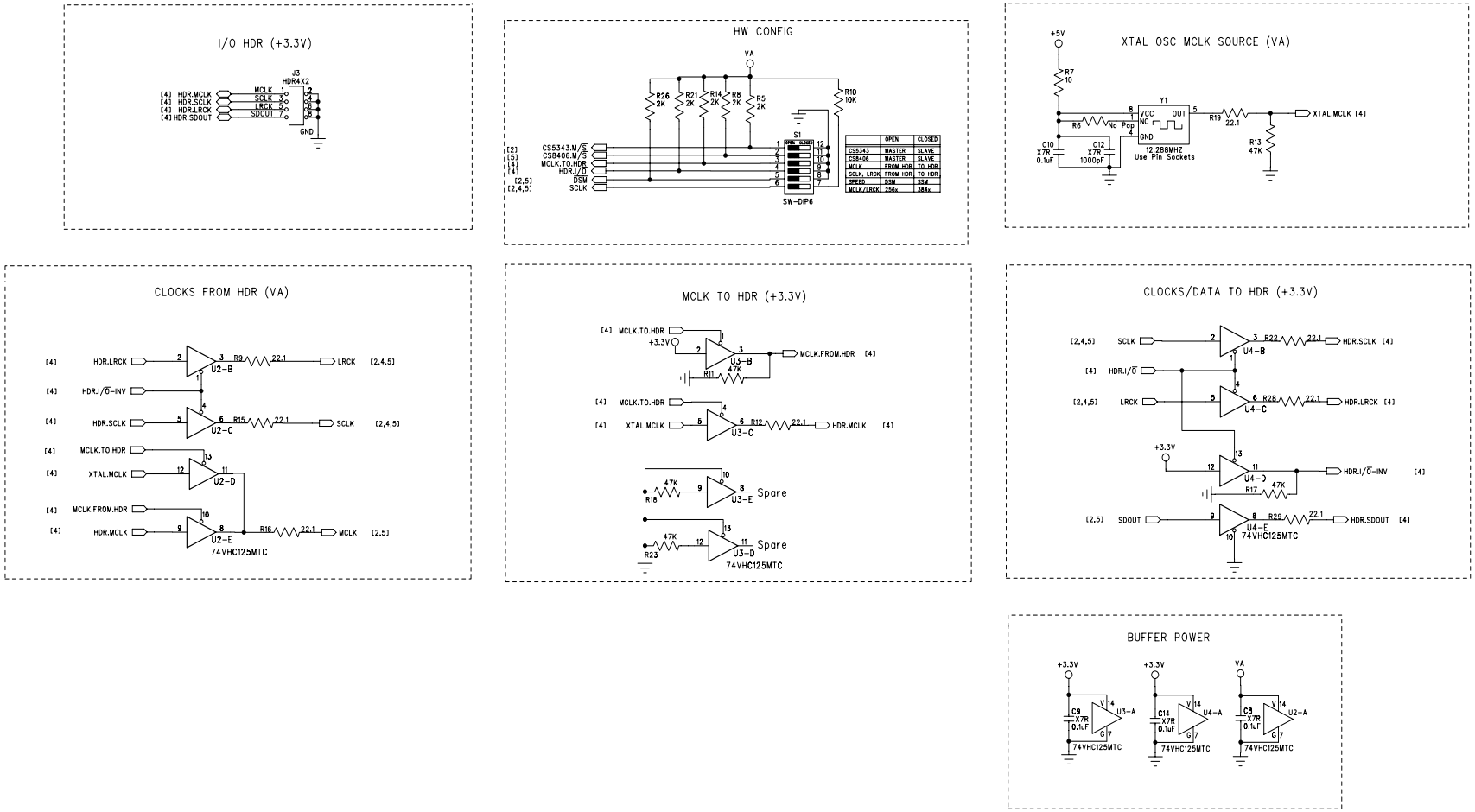


Figure 22. Switches, Crystal Oscillator, and Clock Routing

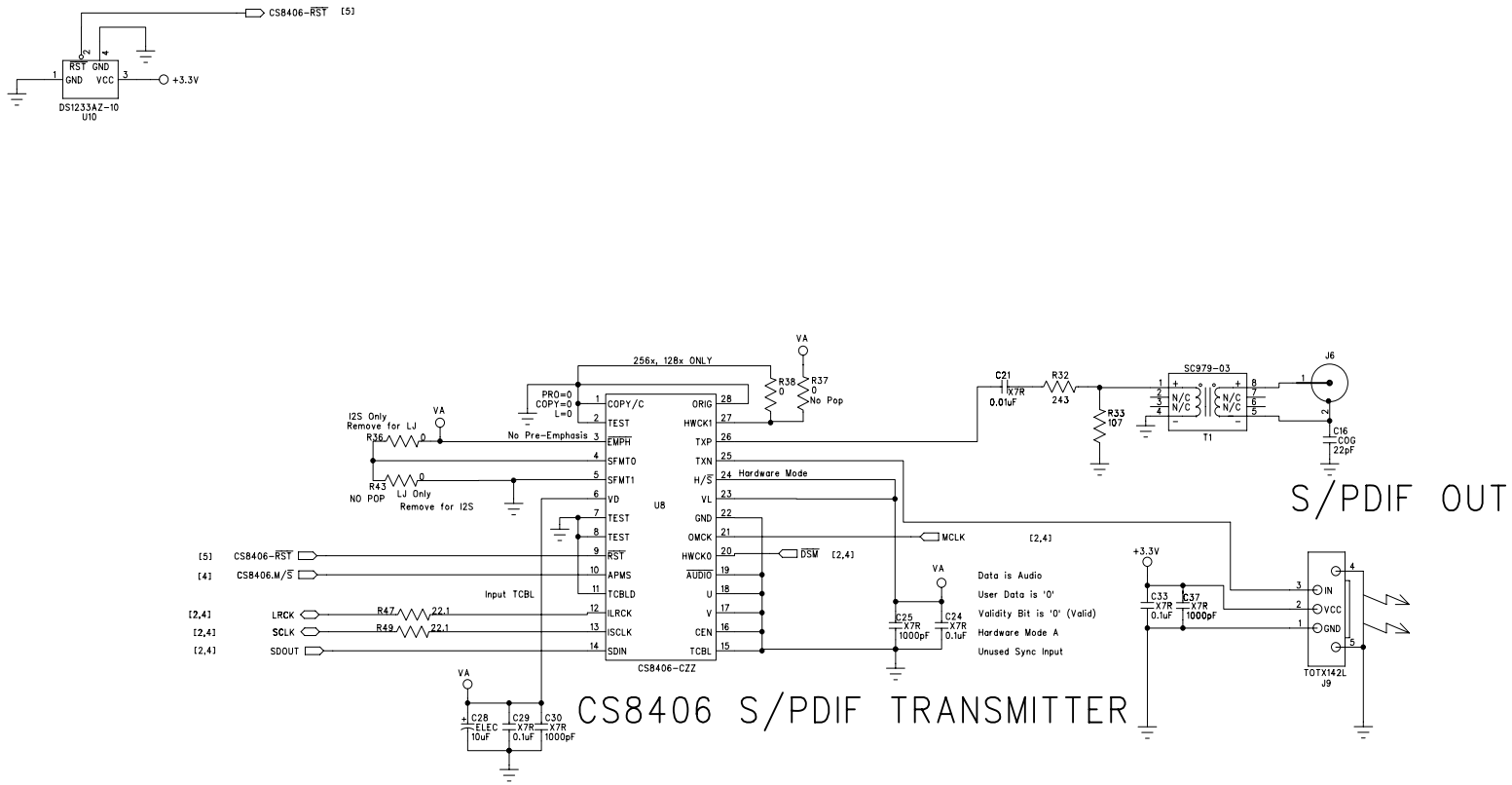


Figure 23. CS8406 S/PDIF Transmitter

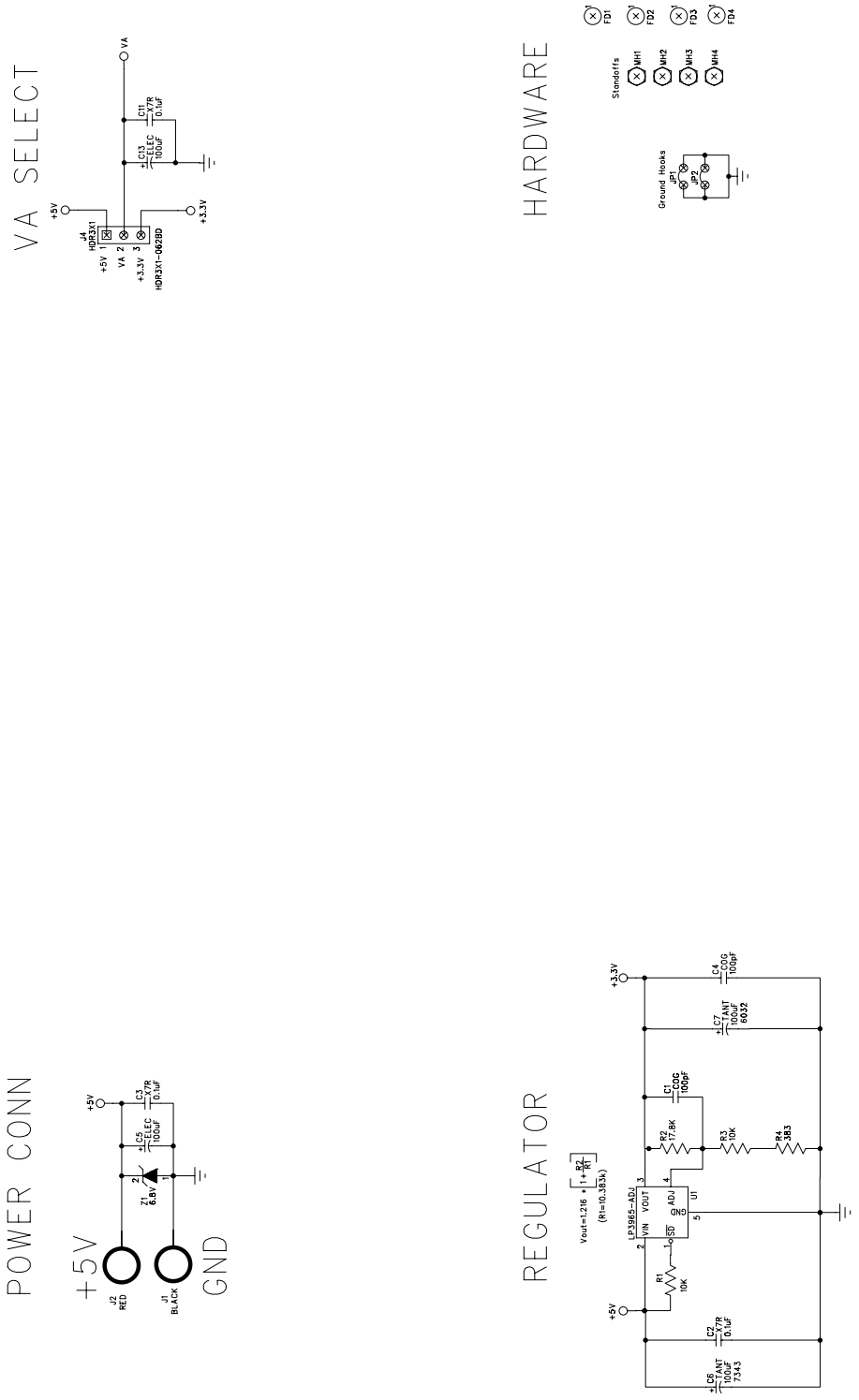


Figure 24. Power

15.CDB LAYOUT

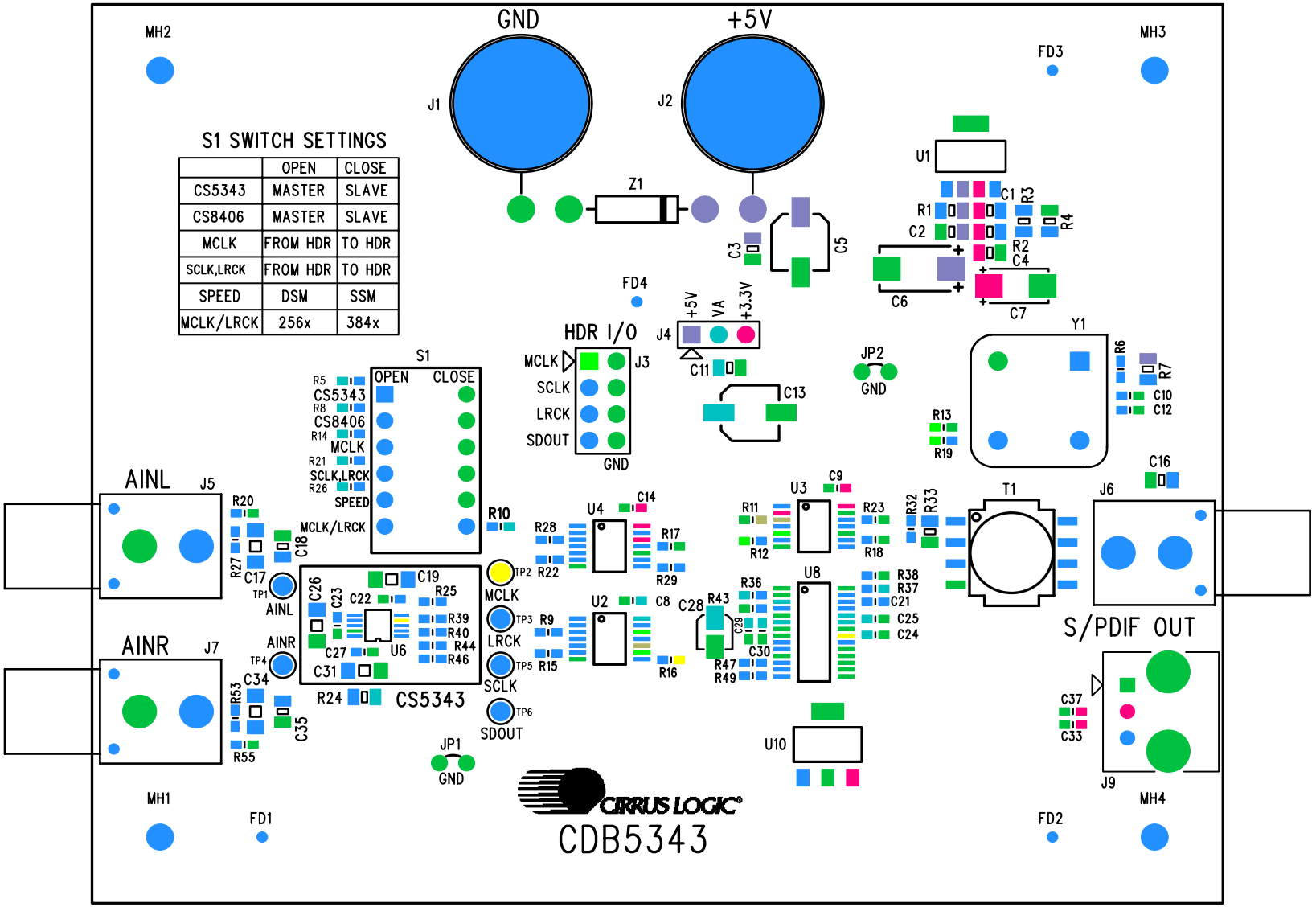


Figure 25. CDB Silk-Screen

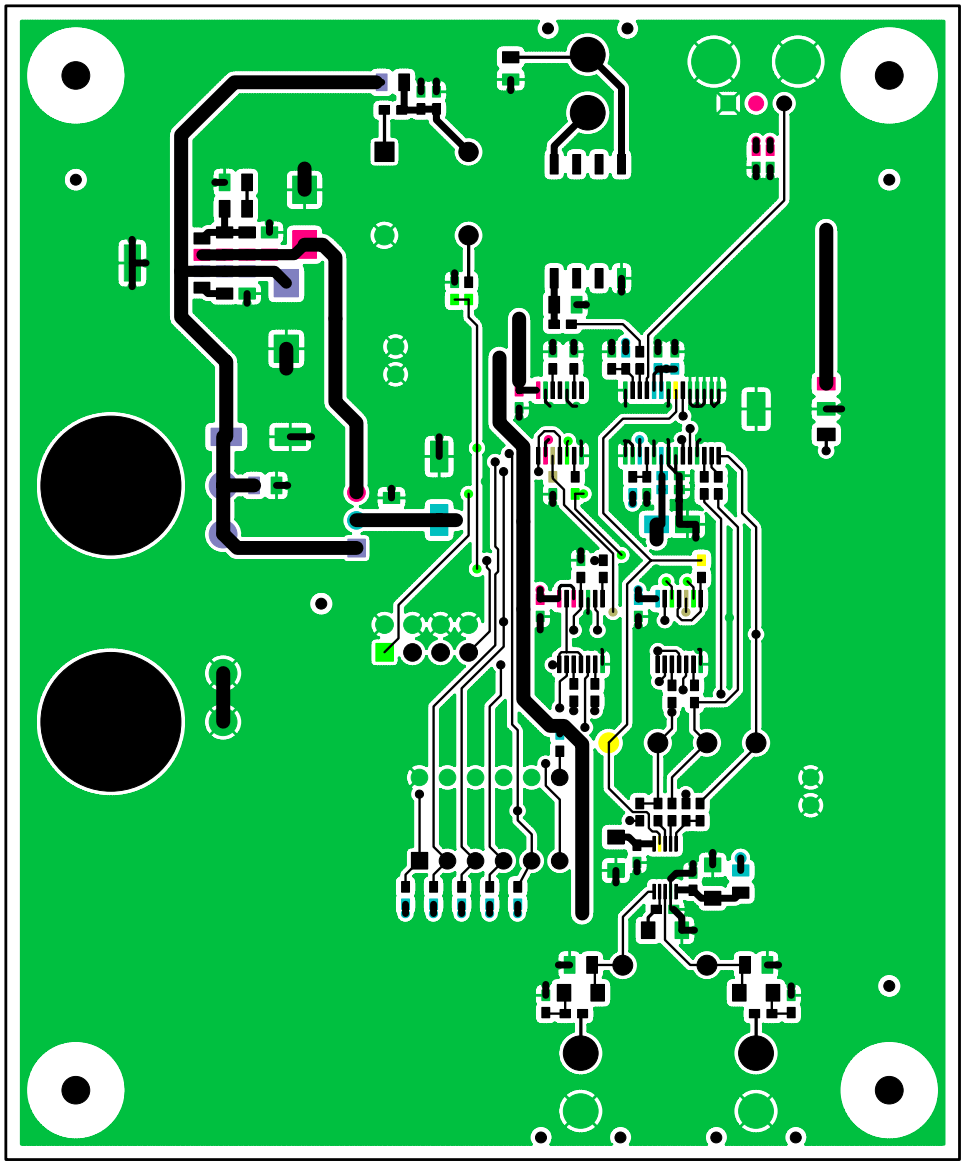


Figure 26. Topside Layer

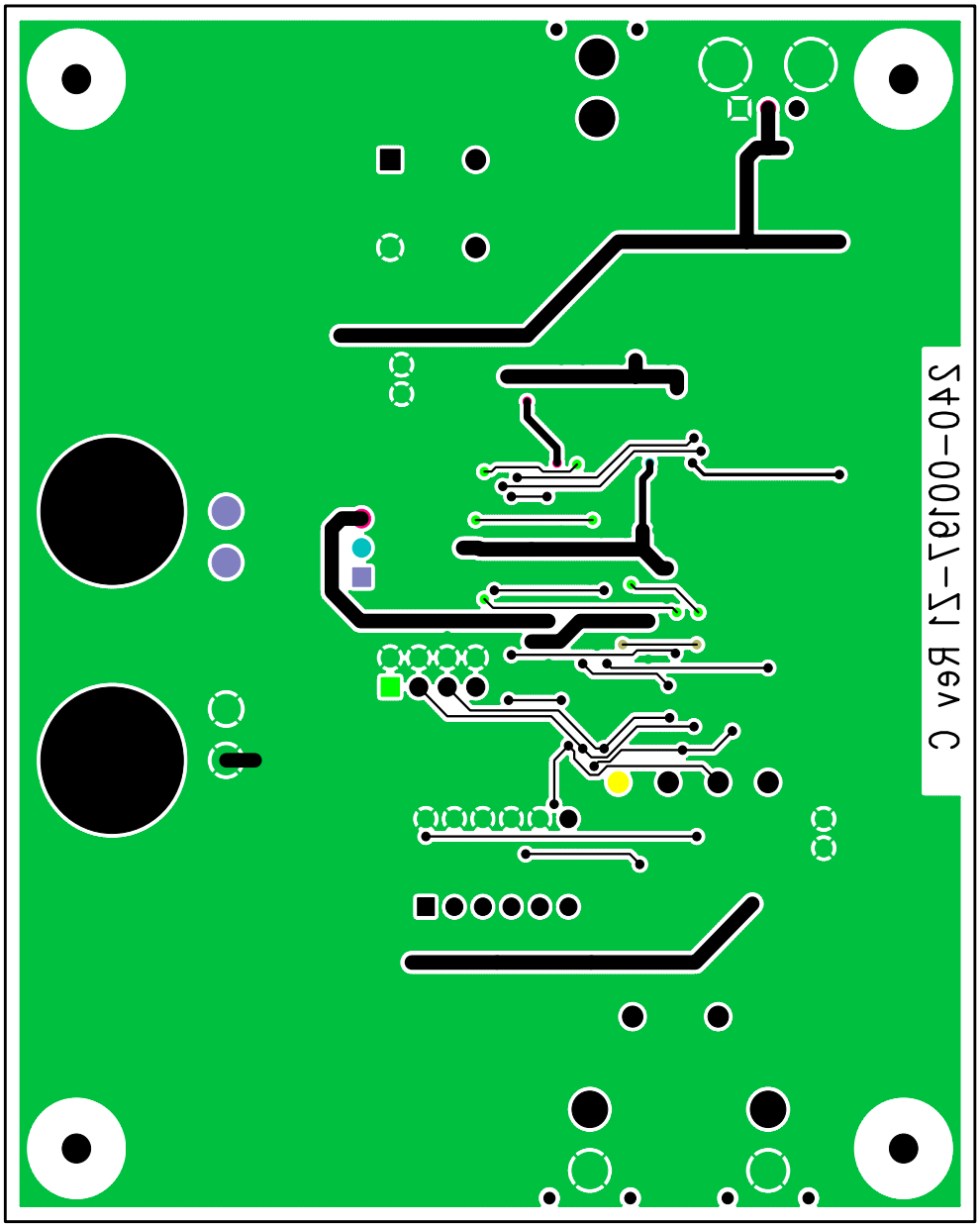


Figure 27. Bottomside Layer

16.REVISION HISTORY

Release	Changes
DB1	Initial Release
DB2	Added Performance Plots

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
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